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RM-6547

B. E. - II (Sem. IV) (IT) Examination

May / June – 2010

Digital Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 2 (Sem. 4) (IT)

Name of the Subject :

☛ Digital Circuits

☛ Subject Code No. : 6 5 4 7 ☛ Section No. (1, 2,.....) : 1&2

Seat No. :

Student's Signature

(2) Attempt all questions.

(3) Answers to the **two** sections must be written in **separate** answer books.

(4) Figures to the extreme right indicate marks.

(5) Assume necessary data.

(6) Draw logic circuit for design problem.

SECTION - I

1 (a) Answer the following : **10**

(i) What are SOP and POS forms of Boolean Expression?

(ii) What is the difference between weighted and non-weighted code? Explain with illustrations.

(iii) Write the difference between truth table and excitation table.

(iv) What are the advantages of digital systems over analog systems?

(v) Write first 10 decimal digits in base 5.

(b) Do as directed : (any **five**) **10**

(i) Convert $(5C7)_{16}$ and $(756.603)_8$ to decimal.

(ii) Convert decimal 250.5 to base 3, base 4, base 7, base 8 and base 16.

(iii) Show that

$$A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$$

(iv) Multiply $(10110)_2$ with $(10.1)_2$

(v) Reduce using mapping the expression

$\sum m\,(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ and implement it in universal logic.

(vi) Simplify following functions and implement them with NAND logic :

F = (B'+D') (A'+C'+D)(A+B'+C'+D)(A' + B+C'+D')

2 (a) What is K-map? Explain the use of it with example. **8**

(b) What is a PLA? Explain it with example. **7**

OR

(b) What is magnitude comparator? Draw logic diagram of a 4-bit comparator. **7**

3 Do as directed : (any **three**) **15**

(i) Implement the following function with a MUX :

$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$

(ii) Explain Half/Full adder circuits. Also show their NAND gate implementation.

(iii) A circuit receives a 4-bit 5211 BCD code. Design the minimum SOP circuit to detect the decimal numbers 0, 2, 4, 6 and 8.

(iv) A logic equation is given as

F = AB'C + B'CD' + ABC + A'B'CD

(a) Prepare a truth table

(b) Simplify using K-map

(c) Realize using NAND gates.

SECTION - II

4 (a) Answer the following : **10**

(i) What are asynchronous inputs in FFs?

(ii) A circuit with m flip-flops would have _____ states.

(iii) State True/False : A + A = 1

(iv) State True/False : The SET input can use to make Q as 0.

(v) What is State table?

(vi) State True/False The circuit for a DEMUX is basically same as that for a decoder.

(vii) 4×1 multiplexer has_____ input, _____ output and _____ select lines.

(viii) State True/False : "Binary Ripple counter is Asynchronous Counter."

(ix) State True/False : The SET input can use to make Q as 0.

(x) A group of flip-flop sensitive to pulse duration is called_____.

(b) Answer in short : (any **five**) **10**

(i) Write difference between synchronous and asynchronous counter.

(ii) Explain Ripple Counter.

(iii) Explain Master-slave flip-flop.

(iv) Realize X-OR function using NAND logic.

(v) What is a Race condition?

(vi) What is Lock-Out?

5 (a) What is Flip/Flop? Discuss characteristics of various Flip-Flop. 8

(b) Design and implement a synchronous 3-bit up/down counter using JK FFs. 7

OR

(b) WRite a short note on 4-bit bidirectional shift register. 7

6 Do as directed : (any **three**) 15

(i) Design 3-bit Parity Generator and 4-bit Parity Checker.

(ii) Design and implement a mod-6 asynchronous counter using T FFs.

(iii) Design a D counter that goes through states 0,1,2,4,0.....

(iv) Write about Johnson Counter.